**v7.52.0.0**

***(Oct 30th, 2022)***

**IDesignSpec™ (IDS)**

**General Enhancements**

1. B#1928 - Supported “**svheader\_opt=1**” property to remove structs from svheader output. More Details
2. F#18289 - Supported IP-XACT 1.2 input. More Details

# F#21220 - Supported c tests output for chip-inside-chip flow. More Details

1. B#1975 - Supported **svheader\_pkg\_name = “any\_string”** top property for changing the package name in svheader output. More Details
2. B#1988 - Supported  **doc\_repeat\_compact=”b2\_%d”** property for visualising the replicated view of block arrays in the HTML output. More Details

**RTL Enhancements**

1. B#1986 - Supported the feature of adding pragma text for register flops and widgets in verilog output. More Details

**Bug Fixes**

**General**

1. F#21468 - Fixed output generation issue for conversion from IDS-Word to XML and vice-versa in IDS-Batch.
2. F#20435 - Fixed offset calculation issue in IDS-Word output from IDS-Batch.
3. F#21318 - Fixed the fatal issue with temp/svheader.vm in IDS-Batch.
4. B#1994 - Fix for search box not working properly.
5. F#21520 - Fixed the issue of switch -hide\_html\_alt2\_prop\_all in HTMLalt2 output.
6. B#1998 - Fix for big IPXACT file import crash on out of memory after annotation.
7. B#1999 - Fixed the issue of local params property issue in svheader.
8. F#21171 - Fix for Repeated sections getting incorrectly generated in C headers.

**RTL**

1. B#1987 - Fix for the compilation failure issue due to addition of a new line in the external access assign statement.
2. F#21382 - Fixed the duplicate assign statement issue when “registered=false” & “rtl\_hw\_vector=true” properties are used together.
3. F#21343 - Fixed the duplicate code inside the always sensitivity list i.e., ( or negedge reset\_l ) for the external register when "reset\_type" and "field\_reset" property are used together.
4. F#21522 - Fixed the port declaration issue for the increment port when used with “incrwidth” property.
5. B#1995 - Fix for Lint width errors due to the difference in width.
6. B#1996 - Fixed the linting error issue which occurs when we add logic OR on the bus in case of signals greater than 1 bit.
7. B#2000 - Fix with else construct, when reg width is greater than the bus width, then valid0, valid1 created for the transfer of 32-bit data in each valid.
8. F#21056 - Fixed the lint errors issue when using the rd\_data\_stages UPF.
9. F#20427 - Fixed the compilation issue due to parametrized reg file instantiated multiple times in multiple addrmap.
10. F#21055 - Fixed the issue when trying to synthesize the CSR block at 300Mhz.
11. F#21046 - Fixed the VCS compilation error due to delay insertion in RTL.

**UVM**

1. B#1992 - Fix for Incorrect generation of RAL with uvm top property uvm.field\_class.
2. B#1993 - Fix for compilation failure because of few missing classes from the output.
3. B#1997 - Fix for compilation Error when using offset above 58 bits.
4. F#19999 - Fix for missing class definition in generated collaterals.
5. F#21370 - Fixed the compilation error issue due to generation of same callback class multiple time.

**IDS NextGen™ (IDS-NG)**

**Enhancements**

1. G#116- Supported the zoom in and zoom out feature in IDS-NG specification. More Details
2. G#116 - Supported the double slash comment capability in IDS-NG specification. More Details
3. G#116 - Supported the dynamic hinting feature in checker view. More Details

**Bug Fixes**

1. G#115 - Fixed the issue of new rows addition upon clicking on tab button in FSM and reg template.
2. G#115 - Fixed the tab issue in complete-IP templates.
3. G#115 - Fixed the issue of copying/pasting the rows in sequence view.
4. F#21330 - Fixed the issue of generation of a specific view when switching from register view to spreadsheet view.
5. F#21603 - Fixed the issue of offset value getting displayed in decimal format.
6. F#21604 - Fixed the issue of partial description generation in word output from IDS-NG.
7. F#21381 - Fixed the issue of inconsistent description string generation in case of verilog output in IDS-NG.

**SoC-Enterprise™ (SoC-E)**

**Enhancements**

1. F#20999 - Supported "-param" switch in soc\_add API More Details

**Bug Fixes**

1. F#21428 - Fixed the same parameter name issue in different module instances of same module.
2. B#1990 - Fixed the connection missing issue when 2 blocks shared the same port name.
3. F#21525 - Fixed the port name (xxx, zzz) reading issue fixed.
4. F#21536 - Fixed the compile error in localparam when list of parameter is passed.
5. F#21089 - Fix for AXI/AHB/APB Clock and Reset port direction to be input.
6. F#21537 - Fix for space insertion between the net name and the square brackets.
7. F#20967 - Fix for connection width mismatch between input and the generated output.